ABSTRACT

A memory system comprising a semiconductor memory for storing digital data, said memory being connectable to a control device in order to receive an address signal and to make data selected through the output-available address signal. The system is characterised in that it comprises a generating circuit for activating a wait signal to be forwarded to the control device during reading operations in such a way as to indicate the non-availability of the data to be read. The generating circuit is such to deactivate the wait signal, in such a way as to indicate the availability of the data to be read, following a waiting time interval correlated with an effective access time for said memory.